REMARKS

In this Response, the claims have not been amended. Accordingly, this Response does not raise new issues or new considerations. Accordingly, Applicants respectfully request entry and consideration of this Response.

Should the Examiner be of the opinion that this Response does not place the Application in a condition for allowance, Applicants respectfully request an Examiner Interview to expedite prosecution prior to issuance of the next communication from the USPTO.

Claims 25-30 are novel over Miles et al. (5,696,666).

Regarding Claim 25, the Examiner states:

> Miles discloses an integrated circuit package with (25) a substrate (14) having a first surface, an opposite second surface, and central throughhole between the first and second surfaces;
> a plurality of electrically conductive circuit patterns (18) on each of the first and second surfaces of the substrate (14), where the circuit patterns (18) of **each of the first and second surface of the substrate (14) include a plurality of lands**, the circuit patterns of the first surface also include a plurality of bond fingers (26) ...
> a hardened encapsulant (16) within said through hole and covering the semiconductor chip (12) and the bond fingers (26), **wherein the lands of each of the first and second surfaces are outward of a perimeter of the encapsulant (16) (see Figure 1)**; (Office Action, pages 2-3, emphasis added.)

The Examiner's statement is respectfully traversed. Applicants respectfully submit that the Examiner has failed to callout where Miles et al. teaches or suggests **lands on both the upper and lower surface** of the substrate 14. Accordingly, the Examiner has also failed to callout where Miles et al. teaches or suggest "**wherein the lands of each of the first and second surfaces are outward of a perimeter of the encapsulant (16)**" as asserted by the Examiner.

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Specifically, Miles et al. teaches:

> **The die 12 is connected to the surface mount solder pads 24 by means of vias 20 through the printed circuit substrate 14**. After wire bonding, a plastic resin such as a glob top or transfer-molded encapsulant 16 is applied over the die 12 and portions of the substrate 14 forming the PBGA chip carrier 10 shown in FIG. 1. In the preferred embodiment, the perimeter portion of the top side of the substrate is not covered by the encapsulating resin. **Also, in this embodiment, the bottom side of the PCB substrate is not covered with encapsulant**. ... As shown in FIG. 2, a perimeter or peripheral chip carrier typically has surface mount solder pads 24 **on the back side of the PCB substrate** located in array format, but only in 3 to 4 rows around the perimeter of the package, leaving the center of the package free of solder interconnection sites. ... As shown in FIG. 2, the PBGA package may be furnished with bare solder pads 24, or as illustrated in FIG. 1, the solder pads may optionally have solder balls or bumps 13. (Col. 3, lines 11-36, emphasis added.)

For purpose of clarity, Applicants note that FIG. 2 of Miles et al. illustrates the bottom surface of the substrate 14:

> FIG. 2 is an exploded view showing the **bottom surfaces** of an overmolded pad grid array chip carrier in accordance with the present invention. (Col. 1, lines 61-63, emphasis added.)

Thus, Miles et al. teaches surface mount solder pads 24 only on the back (bottom) surface of the substrate 14. Generally, the Examiner has failed to callout where Miles et al. teaches or suggests lands on the front (upper) surface of the substrate 14. More particularly, the Examiner has failed to callout where Miles et al. teaches or suggests lands on the front (upper) surface of the substrate 14 outward of a perimeter of the encapsulant 16. Should the Examiner disagree, Applicants respectfully request clarification as to which

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structure the Examiner is considering the lands and how they are disposed outward of a perimeter of the encapsulant 16.

As set forth in MPEP 2131, eighth edition, Rev. 5, Aug. 2006, page 2100-67:

> TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM

For at least the above reasons, Miles et al. does not teach or suggest:

> A stackable semiconductor package comprising:
> a substrate having a first surface, an opposite second surface, and central throughhole between the first and second surfaces;
> a plurality of electrically conductive circuit patterns on each of the first and second surfaces of the substrate, **wherein the circuit patterns of each of the first and second surfaces of the substrate include a plurality of lands**, the circuit patterns of the first surface also include a plurality of bond fingers, and at least some of the circuit patterns of the first surface are electrically connected through the substrate to some of the circuit patterns of the second surface;
> a semiconductor chip in said throughhole and electrically connected to the bond fingers, wherein the semiconductor chip has a first surface with bond pads thereon, and an opposite second surface, the first surface of the semiconductor chip faces in a same direction as the first surface of the substrate, and the second surface of the semiconductor chip is flush with the second surface of the substrate, wherein the second surface of the semiconductor chip is exposed; and
> a hardened encapsulant within said through hole and covering the semiconductor chip and the bond fingers, **wherein the lands of each of the first and second surfaces are outward of a perimeter of the encapsulant**,

as recited in Claim 25, emphasis added. Accordingly, Claim 25 is allowable over Miles et al. Claims 26-30, which depend from Claim 25, are allowable for at least the same reasons as Claim 25.

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For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

Claims 31-33 are patentable over Miles et al. in view of Akram et al. (6,313,522).

For reasons similar to those discussed above regarding Claim 25, Miles et al. does not teach or suggest:

> A stack of semiconductor packages comprising:
> a first semiconductor package comprising: (a) a substrate having a first surface, an opposite second surface, and central throughhole between the first and second surfaces; (b) a plurality of electrically conductive circuit patterns on each of the first and second surfaces of the substrate, **wherein the circuit patterns of each of the first and second surfaces of the substrate include a plurality of lands**, the circuit patterns of the first surface also include a plurality of bond fingers, and at least some of the circuit patterns of the first surface are electrically connected through the substrate to some of the circuit patterns of the second surface that include respective ones of the lands; (c) a semiconductor chip in said throughhole and electrically connected to the bond fingers, wherein the semiconductor chip has a first surface with bond pads thereon, and an opposite second surface, the first surface of the semiconductor chip faces in a same direction as the first surface of the substrate, and the second surface of the semiconductor chip is flush with the second surface of the substrate, wherein the second surface of the semiconductor chip is exposed; (d) a hardened encapsulant within said through hole and covering the semiconductor chip and the bond fingers, **wherein the lands of each of the first and second surfaces are outward of a perimeter of the encapsulant**; and (e) a plurality of electrically conductive balls, wherein each of the conductive balls is fused to a respective one of the lands of the first surface of the substrate; and
> a second semiconductor package comprising a plurality of second electrically conductive balls, wherein the second semiconductor package is in a stack with the first semiconductor package, and the second electrically conductive balls of the second package each superimpose and are electrically connected to a respective one of the lands of the second surface of the substrate of the first semiconductor package,

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as recited in Claim 31, emphasis added. Akram et al. does not cure this deficiency in Miles et al.

Regarding Akram et al., the Examiner states:

> ... Akram discloses a stack of semiconductor packages with ... (d) **a hardened encapsulant** within said through hole and covering the semiconductor chip and the bond fingers, wherein the lands of each of the first and second surfaces are outward of a perimeter of the encapsulant... (see Figures 2-3); (Office Action, pages 4-6, emphasis added.)

The Examiner's statement is respectfully traversed. Applicants respectfully submit the Examiner has failed to callout where Akram et al. teaches or suggests a hardened encapsulant. To illustrate, regarding FIG. 2 as cited by the Examiner, Akram et al. teaches:

> **The first semiconductor device 20 and the first substrate 14 are mounted on the first surface 12A of the base substrate 12 using a plurality of solder balls 48**. Accordingly, the base substrate bond pads 29, the first semiconductor bond pads 26 and the first substrate bond pads 36 are preferably positioned so that each respective bond pad pair is aligned perpendicularly. The solder balls 48 are positioned between corresponding pairs of bond pads 26, 29 and 36, 29 so that the first semiconductor device 20 and the first substrate 14 are electrically and physically coupled to the base substrate 12. The first substrate 14 is positioned so that the first semiconductor device 20 is positioned within the cavity 14C. As the first semiconductor device 20 is positioned within the cavity 14C, the relative height of the semiconductor device/substrate stack is relatively small. Further, the thickness of the solder balls 48 is reduced compared to a stack in which the substrate must extend completely over the semiconductor device. **The second semiconductor device 22 and the second substrate 16 are similarly mounted on the second surface 14B of the first substrate 14 using a plurality of solder balls 49 while the third semiconductor device 24 and the third substrate 18 are mounted on the second surface 16B of the second substrate 16 using a plurality of solder balls 50**. (Col. 10, line 54 to col. 11, line 9, emphasis added.)

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Applicants note the lack of any mention of a hardened encapsulant in the above citation of Akram et al. Should the Examiner disagree, Applicants respectfully request clarification as to which structure the Examiner is considering as the hardened encapsulant.

Accordingly, neither Miles et al., nor Akram et al., either alone or in combination, teach or suggest a stack of semiconductor packages as recited in Claim 31.

Thus, Claim 31 is allowable over Miles et al. in view of Akram et al. Claims 32-33, which depend from Claim 31, are allowable for at least the same reasons as Claim 31.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

Conclusion

Claims 25-33 are pending in the application. For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant(s).

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 24, 2006.

Attorney for Applicant(s) — October 24, 2006 Date of Signature

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